



ATTORNEY DOCKET NO. 28951.5186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Confirmation No.: 4222

Takaki YOSHIDA et al.

Group Art Unit: 2133

Serial No.: 09/697,305

Examiner: Joseph D. Torres

Filed: October 27, 2000

For: FAULT DETECTING METHOD AND
LAYOUT METHOD FOR SEMICONDUCTOR
INTEGRATED CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Customer Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Prior to the continued examination of the above-identified application, please amend the
application as follows: